R15

Code No: 125AH

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, January/February - 2023

IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART - A

(25 Marks)

1.a)	How the size and complexity of ICs are increased day by day?	[2]
b)	What are the advantages of Integrated circuits over discrete components?	[3]
c)	Define a input offset current.	[2]
d)	Write all ac and dc characteristics of op-amp.	[3]
e)	How active filters are differ from passive filters?	[2]
f)	What is the basic principle of oscillator?	[3]
g)	Define a duty cycle of IC555 timer as an astable multivibrator.	[2]
h)	What are the applications of PLL?	[3]
i)	Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?	[2]
j)	Which is the fastest ADC and why?	[3]

PART - B

(50 Marks)

2.a)	Compare various logic families in terms of propagation delay, fan-in, fan-out, Noise margin and power dissipation.	
b)	What are the advantages of CMOS transmission gate?	[6+4]
	OR	
3.a)	Draw the circuit diagram of tristate TTL NAND gate and explain its working.	
b)	How to interface a TTL gate to CMOS gate?	[6+4]

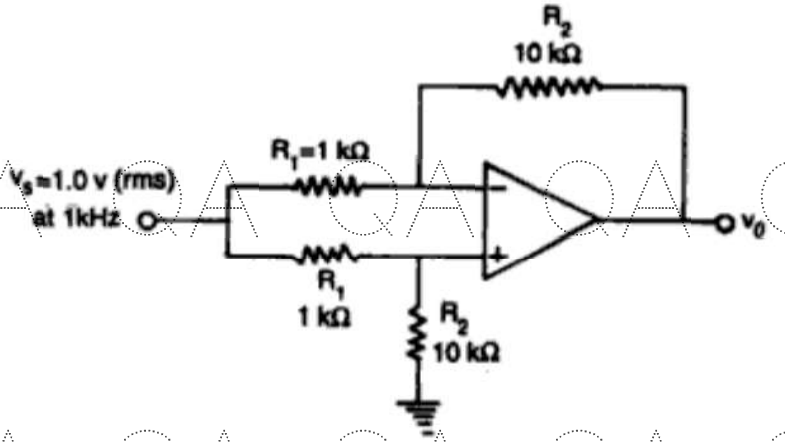
4.a) Design a non-inverting amplifier with a gain of 10.

b) For the figure shown below,

i) Find v_0 if CMRR = 100dB at 1kHz?

ii) Find v_0 resulting from 1% mismatches between the two R_1 resistors?

iii) Find v_0 resulting from 1% mismatches between the two R_2 resistors? [4+6]



OR

5.a) Draw the circuit diagram of sample and hold circuit using op-amp and explain its working.

b) How op-amp is used for integrator? Explain with neat circuit diagram. [5+5]

6. Design a wide band reject filter having $f_h = 400Hz \; and \; f_l = 2kHz$ having pass band gain as 2. Draw its filter response and explain how it working. [10]

OR

7. Design a square wave oscillator for f=1 kHz. The op-amp is a IC741 with supply voltages $\pm 15V$. Draw circuit and explain its working with neat waveforms. [10]

8.a) Draw and explain the functional block diagram of IC 555 timer.

b) Design a symmetrical square waveform generator of 10 kHz using IC 555. [5+5]

OR

9.a) A Schmitt trigger with the upper threshold level $V_{UT} = 0V$ and hysteresis width $V_H = 0.2V$ converts a 1 kHz sine wave of amplitude 4Vpp into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

b) Draw the basic block diagram of VCO and explain the function of each block. [5+5]

10.a) If a 10-bit D/A converter spans a range of 0 to 10V and is always with in 1mV of its ideal output. What is its linearity as a percent of full-scale range?

b) Design a 6-bit inverted R-2R ladder DAC and explain its conversion procedure with neat circuit diagram. [4+6]

OR

11.a) The analog input signal ranges for -5 to +8V in a nine bit A/D converter. What binary number will be produced when analog input is zero?

b) Explain the working of successive approximation ADC with neat circuit diagram. [5+5]

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